

ABSTRACT OF THE DISCLOSURE

an FED cathode plate with internal via includes an internal via; a second dielectric layer; a second gate line; a metal layer 12 covering the gate line and the internal via; and a contact. The internal via is located on a typical tape line. The second dielectric layer is located on the tape line and abutted against the internal via, thereby connecting to an anode by an adhesive. The second gate line is located on the second dielectric layer and abutted against the internal via. The metal layer is covered over the first gate line, the internal via, and the second gate line; and the contact is located on the tape line and connected adjacent to the second dielectric layer, thereby electrically connecting a lead to outside.

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